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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,597	11/28/2003	Osamu Suzuki	520.43306X00	8275
20457 7590 09/03/2009 ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-3873				
EXAMINER LEWIS, MONICA				
ART UNIT 2838		PAPER NUMBER		
NOTIFICATION DATE 09/03/2009		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/722,597

Applicant(s)

SUZUKI ET AL.

Examiner

Monica Lewis

Art Unit

2894

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 August 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4-14 and 21-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4-14 and 21-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/808)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the request for continued examination filed August 17, 2009.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/17/09 has been entered.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 4-14 and 21-24 objected to because of the following informalities: a) please remove the word "formed" because the claims are not directed to the method. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4-9, 11, 12, 14 and 21-24 are rejected under 35 U.S.C. 103(a) as obvious over Zuo (U.S. Patent No. 6,631,077) in view of *Microchip Fabrication* by Peter Van Zant and Ohashi et al. (Japanese Publication No. 07-286788).

In regards to claim 4, Zuo discloses the following:

a) a circuit forming layer (170), on which a plurality of circuits are formed, being formed at a first main surface of an integrated circuit (IC) board (160), said first main surface corresponding to the first principal surface side of the plate-like semiconductor chip (For Example: See Figure 1);

b) driving means of an operating fluid being formed at a second main surface of said IC board, opposite that of said first main surface (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35); and

c) a heat transfer layer (110) being made of a material similar to that of said IC board and connected with the IC board in one body, said heat transfer layer having an outer surface and an opposing inner surface, the outer surface thereof corresponding to the second principal surface side of the plate-like semiconductor chip and in which there is formed between said inner surface and said second main surface of the IC board a closed flow passage, an operating fluid being hermetically enclosed within the closed flow passage (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35);

d) wherein said driving means of the operating fluid is made of a resistor layer (111) and is outside the closed flow passage of said operating fluid (For Example: See Figure 1).

In regards to claim 4, Zuo fails to disclose the following:

a) a plural number of circuits.

However, Van Zant discloses the use of logic and memory elements in a circuit (For Example: See Page 543). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of logic and memory elements as disclosed in Van Zant because it is well known that every integrated circuit contains both logic and memory sections (For Example: See Page 543).

Additionally, since Zuo and Van Zant are both from the same field of endeavor (semiconductor), the purpose disclosed by Van Zant would have been recognized in the pertinent art of Zuo.

b) the resistor layer being electrically operated to give vibration to the hermetically enclosed operating fluid.

However, Ohashi et al. ("Ohashi") discloses the use of a driving means being electrically operated to give vibration to the hermetically enclosed operating fluid (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of a driving means being electrically operated to give vibration to the hermetically enclosed operating fluid as disclosed in Ohashi because it aids in providing control of the heat transporting capacity (For Example: See Abstract).

Additionally, since Zuo and Ohashi are both from the same field of endeavor (semiconductor), the purpose disclosed by Ohashi would have been recognized in the pertinent art of Zuo.

In regards to claim 5, Zuo discloses the following:

a) the resistor layer is disposed in a region where heat generation density is lower than an average of heat generation density of said integrated circuit chip as a whole (For Example: See Figure 1).

In regards to claim 6, Zuo discloses the following:

a) operating fluid is water (For Example: See Table 1).

In regards to claim 7, Zuo fails to disclose the following:

a) plate-like semiconductor chip includes logic elements and memory elements are formed separately within said first principal surface thereof.

However, Van Zant discloses the use of logic and memory elements (For Example: See Page 543). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of logic and memory elements as disclosed in Van Zant because it is well known that every integrated circuit both logic and memory sections (For Example: See Page 543).

Additionally, since Zuo and Van Zant are both from the same field of endeavor (semiconductor), the purpose disclosed by Van Zant would have been recognized in the pertinent art of Zuo.

In regards to claim 8, Zuo discloses the following:

a) the closed flow passage in said heat transfer layer is configured as a plurality of closed flow passages formed between said inner surface of the heat transfer layer and the second main surface of the IC board (For Example: See Figure 1).

In regards to claim 9, Zuo discloses the following:

a) each of said the plurality of closed flow passages has a separate means for driving the operating fluid enclosed within an inside thereof (For Example: See Figure 1)(Note: Applicant discloses that the resistor layer is the heating/driving means (See Specification Page 20 Lines 1 and 2)).

In regards to claim 11, Zuo discloses the following:

a) another closed flow passage (140) which is between said inner surface of the heat transfer layer and said second main surface of the IC board crossing over said plurality of closed flow passages (For Example: See Figure 1).

In regards to claim 12, Zuo discloses the following:

a) each of said plurality of closed flow passages has a separate said means for driving the operating fluid enclosed within an inside thereof (For Example: See Figure 1)(Note: Applicant discloses that the resistor layer is the heating/driving means (See Specification Page 20 Lines 1 and 2)).

In regards to claim 14, Zuo discloses the following:

a) an integrated circuit (IC) board (160) the first main surface corresponding to the first principal surface side of the plate-like semiconductor chip (For Example: See Figure 1);

b) driving means of an operating fluid being formed at a second main surface of said IC board, opposite that of said first main surface (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35); and

c) a heat transfer layer (110) being made of a material similar to that of said IC board and integrated with the IC board in one body, for suppressing a local increase of temperature caused by heat generation of circuits within said IC board, said heat transfer layer having an outer surface and an opposing inner surface, the outer surface thereof corresponding to the second principal surface side of the plate-like semiconductor chip and in which there is formed between said inner surface and said second main surface of the IC board a closed flow passage (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35);

d) wherein said driving means of the operating fluid is made of a resistor layer (111) (For Example: See Figure 1).

In regards to claim 14, Zuo fails to disclose the following:

a) a plural number of circuits.

However, Van Zant discloses the use of logic and memory elements in a circuit (For Example: See Page 543). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of logic and memory elements as disclosed in Van Zant because it is well known that every integrated circuit contains both logic and memory sections (For Example: See Page 543).

Additionally, since Zuo and Van Zant are both from the same field of endeavor (semiconductor), the purpose disclosed by Van Zant would have been recognized in the pertinent art of Zuo.

b) the resistor layer being electrically operated to give vibration to the hermetically enclosed operating fluid.

However, Ohashi discloses the use of a driving means being electrically operated to give vibration to the hermetically enclosed operating fluid (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of a driving means being electrically operated to give vibration to the hermetically enclosed operating fluid as disclosed in Ohashi because it aids in providing control of the heat transporting capacity (For Example: See Abstract).

Additionally, since Zuo and Ohashi are both from the same field of endeavor (semiconductor), the purpose disclosed by Ohashi would have been recognized in the pertinent art of Zuo.

In regards to claims 21 and 24, Zuo discloses the following:

a) both said plate like semiconductor chip and said heat transfer layer are made of a material of silicon (For Example: See Column 1 Line 14 and Column 4 Lines 43-54).

In regards to claim 22, Zuo discloses the following:

a) a circuit forming layer (170), being formed at a first main surface of an integrated circuit (IC) board (160), said first main surface corresponding to the first principal surface side of the plate-like semiconductor chip (For Example: See Figure 1);

b) driving means of an operating fluid being formed at a second main surface of said IC board, opposite that of said first main surface (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35); and

c) a heat transfer layer (110) being made of a material similar to that of said IC board and connected with the IC board in one body, said heat transfer layer having an outer surface and an opposing inner surface, the outer surface thereof corresponding to the second principal surface side of the plate-like semiconductor chip and in which there is formed between said inner surface and said second main surface of the IC board a closed flow passage, an operating fluid being hermetically enclosed within the closed flow passage (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35);

In regards to claim 22, Zuo fails to disclose the following:

- a) a plural number of circuits.

However, Van Zant discloses the use of logic and memory elements in a circuit (For Example: See Page 543). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of logic and memory elements as disclosed in Van Zant because it is well known that every integrated circuit contains both logic and memory sections (For Example: See Page 543).

Additionally, since Zuo and Van Zant are both from the same field of endeavor (semiconductor), the purpose disclosed by Van Zant would have been recognized in the pertinent art of Zuo.

In regards to claim 23, Zuo discloses the following:

- a) an integrated circuit (IC) board (160) the first main surface corresponding to the first principal surface side of the plate-like semiconductor chip (For Example: See Figure 1);

- b) driving means of an operating fluid being formed at a second main surface of said IC board, opposite that of said first main surface (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35); and

- c) a heat transfer layer (110) being made of a material similar to that of said IC board and integrated with the IC board in one body, for suppressing a local increase of temperature caused by heat generation of circuits within said IC board, said heat transfer layer having an outer surface and an opposing inner surface, the outer surface thereof corresponding to the second principal surface side of the plate-like semiconductor chip and in which there is formed between said inner surface and said second main surface of the IC board a closed flow passage (For Example: See Figure 1, Column 1 Line 14, Column 4 Lines 43-54 and Column 5 Lines 19-35);

- d) wherein said driving means of the operating fluid is made of a resistor layer (111) (For Example: See Figure 1).

In regards to claim 23, Zuo fails to disclose the following:

- a) a plural number of circuits.

However, Van Zant discloses the use of logic and memory elements in a circuit (For Example: See Page 543). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of logic and memory elements as disclosed in Van Zant because it is well known that every integrated circuit contains both logic and memory sections (For Example: See Page 543).

Additionally, since Zuo and Van Zant are both from the same field of endeavor (semiconductor), the purpose disclosed by Van Zant would have been recognized in the pertinent art of Zuo.

7. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as obvious over Zuo (U.S. Patent No. 6,631,077) in view of *Microchip Fabrication* by Peter Van Zant, Ohashi et al. (Japanese Publication No. 07-286788) and O'Connor et al. (U.S. Publication No. 2002/0039280).

In regards to claim 10, Zuo fails to disclose the following:

- a) a plurality number of temperature detecting means which are provided within said semiconductor chip, wherein the plural driving means which provided for the plural closed flow passages, respectively are controlled in dependence on temperature detection outputs from said temperature detecting means.

However, O'Connor et al. ("O'Connor") discloses the use of temperature detection means (For Example: See Page 8-Claim 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of temperature detecting means as disclosed in O'Connor because it aids in providing a means to allow the device to be cooled (For Example: See Abstract).

Additionally, since Zuo and O'Connor are both from the same field of endeavor (semiconductor), the purpose disclosed by O'Connor would have been recognized in the pertinent art of Zuo.

In regards to claim 13, Zuo fails to disclose the following:

a) a plurality number of temperature detecting means which are provided within said semiconductor chip, wherein the plural driving means which provided for the plural closed flow passages, respectively are controlled in dependence on temperature detection outputs from said temperature detecting means.

However, O'Connor discloses the use of temperature detection means (For Example: See Page 8-Claim 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Zuo to include the use of temperature detecting means as disclosed in O'Connor because it aids in providing a means to allow the device to be cooled (For Example: See Abstract).

Additionally, since Zuo and O'Connor are both from the same field of endeavor (semiconductor), the purpose disclosed by O'Connor would have been recognized in the pertinent art of Zuo.

Response to Arguments

8. Applicant's arguments filed 8/17/09 have been fully considered but they are not persuasive. First, Applicant argued that Zuo failed to disclose that "the heat spreader, the driving means as well as the closed flow passage would be directly formed on the opposing side of an IC board, such as the second main surface of the IC board." However, Applicant is arguing limitations that are not disclosed in the claims. The claims do not state that they are "directly formed" on the opposing sides of the IC board.

Finally, Applicant argues that “a skilled artisan would not have been led to modify Zuo’s assembly in a way that would have achieved the present invention, based upon the combined teachings of Zuo and the above-named references.” However, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant’s disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-272-8300 for regular and after final communications.

/Monica Lewis/
Primary Examiner, Art Unit 2894

September 1, 2009